

Characterization of high performance CNT-based TSV for high-frequency RF applications

Sukeshwar Kannan^{*1}, Bruce Kim¹, Anurag Gupta¹, Seok-Ho Noh² and Li Li³

¹University of Alabama, Tuscaloosa, Alabama, 35487-0286 USA

²Andong National University, South Korea

³Cisco Systems, Inc., USA

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Abstract. In this paper, we present modeling and characterization of CNT-based TSVs to be used in high-frequency RF applications. We have developed an integrated model of CNT-based TSVs by incorporating the quantum confinement effects of CNTs with the kinetic inductance phenomenon at high frequencies. Substrate parasitics have been appropriately modeled as a monolithic microwave capacitor with the resonant line technique using a two-polynomial equation. Different parametric variations in the model have been outlined as case studies. Furthermore, electrical performance and signal integrity analysis on different cases have been used to determine the optimized configuration for CNT-based TSVs for high frequency RF applications.

Keywords: TSV; CNT; modeling; signal integrity; high-frequency; RF applications

1. Introduction

For 3D integration, Through Silicon Via has been rapidly evolving as a key enabler technology. The increasing complexity and functionality of large-scale integrated systems demand new innovations in the interconnect domain to keep pace with the rapidly transforming electronic component and packaging industry. There is an imminent need for on-chip interconnects and packaging to converge with optimizing circuit performance in terms of signal integrity, power management and thermal dissipation (Zhu *et al.* 2010). As per guidelines outlined in ITRS 2008 (*International Technology Roadmap for Semiconductors 2008 Ed*), the upcoming challenges are to integrate heterogeneous and independent technologies such as analog, digital and RF into one single system; invariably, TSV interconnects have shown great promise to bring us closer to this goal.

Through Silicon Vias, as 3D interconnects, are attractive candidates for future LSI architectures due to their inherent capability to overcome the fundamental bottlenecks associated with conventional interconnects. They have provided much-needed physical size reduction in the “More than Moore” era of LSI architectures, along with faster operating speeds. The short interconnect length is not only beneficial for improving clock rates and delay but is also efficient in terms of power consumption. However, despite the aforementioned advantages, there are critical issues such

*Corresponding author, Graduate Research Assistant, E-mail: skannan@crimson.ua.edu

as choice of filler materials, innovative design solutions, and electrical and thermal issues, which need to be resolved prior to a large scale commercialization of TSV technology. Therefore, academia and industry are devoting rigorous research to various aspects in these domains. We believe that the most critical aspect for achieving heterogeneous compatibility of RF, analog and digital technology on the same system through TSVs is the choice of filler material used in these vias. Signal integrity and transmission characteristics are the deciding factor of the commercial success of any technology, and the extent to which the filler material can influence the performance of the system is non-intuitive. The desired properties of via-filling material are high current density transmission, void-free filling, high resistance to thermal fatigue and low stress levels during operation. Hence, it is easy to recognize the importance of filler material for complete high-end performance of the stacked die. It is thus of utmost importance to investigate filler materials for TSVs that can maintain high standards in all aforementioned domains. Previously, we investigated Single Walled-Carbon Nanotubes (SW-CNT) as an excellent choice for filler material (Gupta *et al.* 2010). Conventionally, copper (Cu) is widely used as filler material due to its economic feasibility and technical superiority. In fact, high electrical conductivity, mature deposition technology and good thermal properties make Cu an excellent choice. However, limitations in achieving Physical Vapor Deposition (PVD), seed layer deposition for Electro-Chemical Deposition (ECD), problems of electro-migration and increasing resistivity due to combined size and scattering effects at micro level make Cu a difficult choice for high-aspect ratio vias (Steinhogel *et al.* 2005). It has been found that for relatively low frequencies (~ 10 GHz), SW-CNT bundles are indeed a good choice; however, it is still of significant interest to investigate the behavior of CNT-based TSVs for relatively high RF frequencies such as those used for radar applications. We have also previously found in our model of CNT-based TSV for low frequencies that SW-CNT bundles offer tremendous performance-based benefits such as excellent current carrying capability ($>10^{10}$ A/cm², three orders of magnitude higher than Cu), negligible electro-migration and good thermal stability. However, to our knowledge there is no significant empirical evidence demonstrating the performance of CNT-based TSVs at RF frequencies.

In this work, we investigate an improvised integrated model of CNT-based TSVs for RF frequencies by taking into consideration substrate effects and kinetic inductance contribution of various parasitics, in addition to the quantum mechanical transport effects in-these 1D mesoscopic systems.

2. Approach

CNTs are nanostructures that exhibit quantum mechanical transport effects and must be analyzed for effective implementation in TSVs. To obtain an optimal design solution using CNTs in TSVs, the quantum mechanical parameters that form the parasitics of CNTs in an electrical circuit model are rigorously investigated. To realistically model a CNT-based TSV structure, CNT-based parasitics have been designated as solutions to the Schrödinger wave equation (Datta 1995). Conventionally, copper is used as TSV filler material and exhibits metallic properties, but when copper is replaced by CNTs as the filler material, the interconnect system becomes highly complicated due to the induced quantum mechanical transport effects in these one-dimensional mesoscopic systems, which have to be accounted for in the electrical circuit model. We have developed an integrated electrical circuit model for CNT-based TSVs by considering quantum

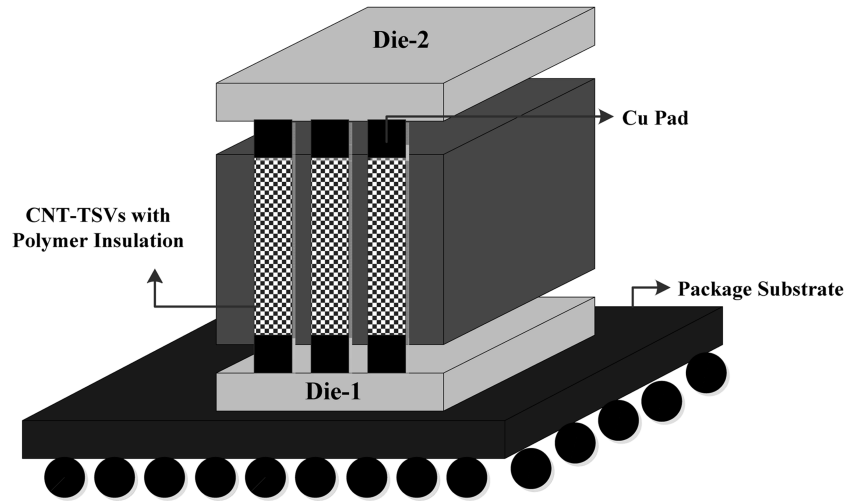


Fig. 1 CNT-based TSV structure for high-frequency RF applications

mechanical transport effects such as quantum resistance, kinetic inductance and quantum capacitance. This model is used for the simulation case studies presented in section 5. Electrical circuit models have been developed for both single-wall CNTs (SW-CNTs) and multi-wall CNTs (MW-CNTs) and this paper presents a comparative study of these two in TSVs for high-frequency RF applications. For high-frequency applications, the major bottleneck is the modeling of TSV itself because several key factors that contribute to the via's electrical performance such as low cost, reliable via formation technologies, proper choice of materials for via filling and innovative design solutions that address electrical and thermal issues remain to be rigorously investigated (Kannan *et al.* 2010, Kim *et al.* 2010). Along with the need for low-cost and high-yield process technology, the successful application of TSV technology should be accompanied by optimal electrical design. The electrical design of TSV interconnections requires careful consideration of complex electrical behavior. Through silicon vias are fabricated in lossy silicon substrates and are exposed to coupling, distortion and additional losses (Han *et al.* 2010). When TSVs are used for high-frequency applications, SiO_2 cannot be used as an insulating layer due to its high fringing capacitance. Instead, a polymer like benzocyclobutane (BCB) is used as an insulating layer, and a conformal coating is achieved through a deep reactive ion etching process. Therefore, it is of utmost importance to obtain an electrical model of TSV by considering various modeling constraints to achieve an optimal design solution. The TSV structure considered for modeling is shown in Fig. 1.

In order to realistically model TSVs for high-frequency RF applications we have developed a substrate-dependent model for TSVs by modeling them as a transmission line including the quantum mechanics transport effects for CNTs and the substrate as a monolithic microwave capacitor. This would enable us to achieve a frequency-dependent model that is very realistic for high-frequency radar applications. At high frequencies, copper exhibits skin effects that increase TSV resistance due to the decrease in current carrying capacity. Therefore, we have chosen CNTs as the filler material because they do not exhibit skin effect at high frequencies. For SW-CNTs we consider quantum mechanical transport effects such as quantum resistance, magnetic inductance and quantum

capacitance; however, for MW-CNTs, kinetic inductance is an additional parasitic parameter included in the electrical circuit model. We have developed the integrated circuit model for SW-CNTs and MW-CNTs discussed in section 4 and performed various case studies by varying the via dimensions, number of CNTs used in the bundle and CNT diameter. We evaluated the CNT performance by analyzing the S -parameters at high frequencies. The signal integrity of CNT-based TSVs was evaluated by performing a time domain analysis to compute the RC-delay using a Time Domain Reflectometer (TDR) and Eye Diagram Analysis for high data rates on the order of 15 to 25 Gbps.

3. Theory

To perform CNT modeling, we need to understand quantum mechanical transport effects. We make certain assumptions to help understand the model parasitics associated with these nanostructures. Although explicit derivations of these quantities have been omitted and only the final formulae have been incorporated for calculation purposes, interested readers may look up the references provided (Naeemi and Meindl 2009, Datta 2004).

3.1 CNT quantum resistance

CNT quantum resistance is the minimum resistance of a quantum wire neglecting any scatterings at the contacts or along the nanowire. According to the theory of Landauer-Buttiker (Avron *et al.* 2004), the maximum conductance that can be achieved by CNT assuming perfect contacts, is $4e^2/h=155 \mu S$, which takes into account the spin degeneracy and sub-lattice degeneracy of electrons in graphene. It should be noted that this value of conductance holds for ballistic CNT where the mean free path of electrons (λ) (typically $> 1 \mu m$) is greater than length of CNT. When the length of CNT exceeds the typical mean free path, additional ohmic resistance due to scattering, which scales with length, has to be taken into consideration and is given by $(h/4e^2) L/\lambda$, L being the length of CNT (Datta 1995).

3.2 CNT kinetic inductance

The total energy associated with electric current is (Datta 2004)

$$E = \int_{allspace} \frac{1}{2} \mu H^2 dV + \int_{conductor} \frac{1}{2} n m v^2 dV \quad (1)$$

where μ is permeability, H is the magnetizing force, and m , v and n are mass, speed, and density of charged particles respectively. In bulk wires, the energy stored in the magnetic field is large enough that the second integral can be safely neglected. However, for 1D structures such as CNTs, kinetic inductance has to be taken into account in certain conditions. For example, kinetic inductance has a significant effect on CNTs under the ballistic transport condition when the length of nanotube (L) is less than the mean free path (λ). This is true because this term has been derived considering no voltage drop across CNT, which is only valid under the ballistic transport condition (Burke 2002). When the length of CNT increases, including kinetic inductance can induce significant errors in calculation. Also, studies on high frequency characteristics have shown that there are no large kinetic inductance effects observed with frequencies up to 10 GHz (Yu and Burke 2005).

3.3 CNT quantum capacitance

According to Burke (2002), quantum capacitance represents stored energy in carbon nanotube that carries current. It can be expressed as $C_Q = 2e^2 / (h v_F)$, where, v_F is the Fermi velocity of CNT ($\approx 8 \times 10^5$ m/s), h is the Planck's constant and e is the electronic charge. Also, as mentioned above, given that CNT has 4 conducting channels in parallel, the effective capacitance per CNT is $4C_Q$, which is taken in series with electrostatic capacitance as the same charge resides on both of them.

3.4 CNT magnetic inductance

For SW-CNTs we ignore the kinetic inductance and consider only the magnetic inductance as a contributing parasitic for the electrical circuit model because the geometric mean difference (GMD) for SW-CNTs is extremely small. However, for MW-CNTs the GMD is 1/4 of its diameter; therefore, kinetic inductance cannot be neglected. Hence, in MW-CNTs we consider both kinetic and magnetic inductances in the electrical circuit model.

Since CNT is a cylindrical structure, its magnetic inductance can be obtained from Greenhouse (1974) by employing the concepts of geometric mean distance and arithmetic mean distance (AMD) as follows

$$L_M = \frac{\mu_0}{2\pi} \cdot L \cdot \left[\ln \left(\frac{L}{S} + \sqrt{1 + \frac{L^2}{S^2}} \right) - \sqrt{1 + \frac{S^2}{L^2}} + \frac{S}{L} \right] \quad (2)$$

3.5 Effective Series Resistance (ESR) and Effective Series Inductance (ESL)

Effective series resistance represents the resistance of TSVs and their inner conductor terminations. The TSVs that transmit signals between two stacked dies are considered transmission lines, and the effective series resistance of the substrate is calculated with the resonant line technique and modeled with a two-polynomial equation. The series resistance of the capacitor is given by Lakshminarayanan *et al.* (2000), Maher *et al.* (1978)

$$R = Z_0 \left[\frac{\pi f L}{4f_0} \cos ec^2 \left(\frac{\pi f}{2f_0} \right) - \frac{1}{2} \cot \left(\frac{\pi f}{2f_0} \right) \right] \cdot \left(\frac{1}{Q_s} - \frac{1}{Q_0} \right) + \frac{\omega L}{Q_s} \quad (3)$$

The resonant line is designed to have a high Q -factor and is given by the classical transmission line theory as in Lakshminarayanan *et al.* (2000), Maher *et al.* (1978)

$$Q = 8.39 b \sqrt{f} \quad (4)$$

where f is the frequency in GHz and b is the inner radius of the TSV, neglecting dielectric loss.

When the Q -factor of the system (Q_s) is small compared to the Q -factor of the TSV, all losses are considered to be due to skin effect in the TSV. The Q -factor at the test frequency (Q_0) is obtained by using the Q -factor (Q_0') at the natural frequency and is given by Lakshminarayanan *et al.* (2000), Maher *et al.* (1978)

$$Q_0 \approx \left(\frac{f}{f_0} \right) Q_0' \quad (5)$$

There is resistive loss in the substrate that is frequency dependent because the current is at its

maximum at odd harmonics and zero at even harmonics. This resistive loss is given by Lakshminarayanan *et al.* (2000), Maher *et al.* (1978)

$$R_0 = 0.004 \left(\frac{f}{f_0} \right)^{0.84} \Omega \quad (6)$$

Combining (3), (5) and (6) we get the effective series resistance of the substrate as Lakshminarayanan *et al.* (2000), Maher *et al.* (1978)

$$ESR = Z_0 \left[\frac{\pi f}{4f_0} \cos e c^2 \left(\frac{\pi f}{2f_0} \right) - \frac{1}{2} \cot \left(\frac{\pi f}{2f_0} \right) \right] \cdot \left(\frac{1}{Q_s} - \frac{1}{Q_0' \sqrt{\frac{f}{f_0}}} \right) + \frac{\omega L}{Q_s} - R_0 \quad (7)$$

The effective series inductance is a function of TSV pitch, and the inductance increases with a decrease in TSV pitch. The effective series inductance is given by Pucel (1981), Benabe (1998)

$$ESL = L_{TSV} \cdot K_g \quad (8)$$

where L_{TSV} is the self-inductance of the TSV and K_g is the correction factor that depends on TSV pitch and the diameter of TSV. The correction factor is given by Pucel (1981), Benabe (1998)

$$K_g = K_{g_a} - K_{g_b} \cdot \ln \left(\frac{r_{via}}{t_{silicon} + t_{polymer}} \right) \quad (9)$$

The coefficients K_{g_a} and K_{g_b} are determined using circuit optimization during the model extraction process for the silicon substrate and insulating polymer layer respectively.

The capacitance of the silicon substrate is given by

$$C_{sil} = \frac{\epsilon_0 \epsilon_r A}{d_{PITCH}} \quad (10)$$

where, $A = \pi r_{via} * H_{TSV}$ is the effective area considered for the capacitance.

The conductance of silicon substrate is given by

$$G_{sil} = \frac{\pi \sigma}{\ln \left(\frac{d_{PITCH}}{2r_{via}} + \sqrt{\left(\frac{d_{PITCH}}{2r_{via}} \right)^2 - 1} \right)} \quad (11)$$

where, σ is the conductivity of the silicon substrate.

Now we are in a position to understand the individual components of the integrated electrical circuit model for SW-CNT- and MW-CNT-based TSVs that we have used for case studies in simulation and characterization.

4. Electrical circuit model

From the theory mentioned in section 3, we understand the quantum mechanics transport effects in these nanostructures. In this section we will discuss the electrical circuit model of SW-CNTs and

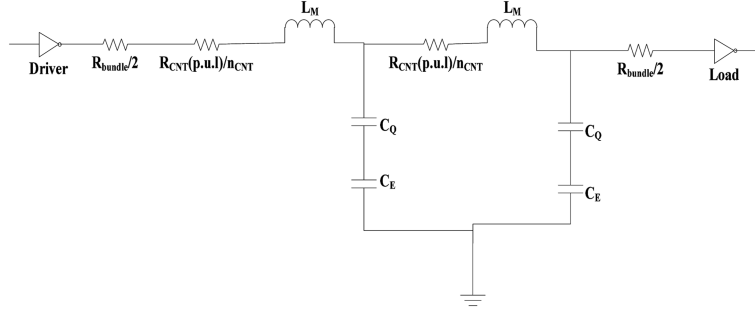


Fig. 2 Electrical model of SW-CNT (Banerjee and Srivastava 2006)

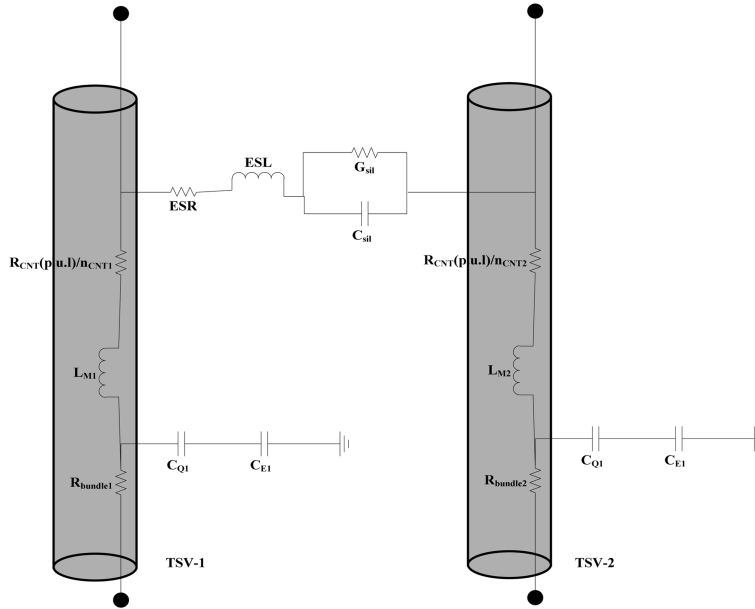


Fig. 3 Equivalent electrical circuit model of two SW-CNT-based TSVs

MW-CNTs and integrate it into the substrate-dependent model of TSVs to achieve an optimal design solution for CNT-based TSVs for high-frequency RF applications.

4.1 Electrical circuit model of SW-CNT-based TSV

We have considered a set of specifications to calculate the parasitic values and obtain the equivalent electrical model. We use SW-CNTs as filler material in the TSV, which would contribute to self-resistances ($R_{bundle/2}$, $R_{CNT(PUL)/n_{CNT}}$) and magnetic inductance (L_M). It also has other parasitic capacitances such as quantum capacitance (C_Q) and electrostatic capacitance (C_E), as shown in Fig. 2.

Height of the CNT ($h_{CNT} = h_{TSV}$) = 90 μm ; diameter of each individual CNT (d_{CNT}) = 1 nm; distance of CNT to ground plane (y) = 100 μm ; λ_{CNT} (typical mean free path of electrons in CNT) = 1.6×10^{-6} μm ; number of CNT in the bundle (n_{CNT}) = 37522, which we approximated by calculating

the area of the via. Using the diameter of the CNT, we then used a lower number by considering the minimum density of metallic SW-CNT; we increased this number for different case studies in our simulations. The equivalent electrical circuit model of SW-CNT-based TSV is as shown in Fig. 3.

The resistance of the SW-CNT is computed from the following

$$R_{Bundle} = \frac{R_F}{n_{CNT}} \quad (12)$$

where $R_F = \frac{h}{4e^2} = 6.45 \text{ k}\Omega$, is the fundamental resistance of the CNT as described earlier in the paper

where h is the Planck's constant and e is electronic charge. Since the length of CNT $>$ typical mean free path of electrons we have to use

$$R_{CNT} = \frac{R_F \cdot h_{CNT}}{\lambda_{CNT}} \quad (13)$$

This takes care of the scattering occurring in the CNT as described above.

$$\text{Quantum capacitance } C_Q = \frac{2e^2}{h\nu_F} \quad (14)$$

assuming ν_F as the typical Fermi velocity of electrons in the carbon nanotube to be $8 \times 10^5 \text{ m/s}$.

Electrostatic capacitance of the bundle is given by the following equation

$$C_E = 2C_{En} + \frac{(n_w - 2)}{2} \cdot C_{Ef} + \frac{3(n_H - 2)}{5} \cdot C_{En} \quad (15)$$

where C_{En} and C_{Ef} are the parallel plate capacitances of isolated SW-CNT with respect to near and far neighboring interconnects respectively, and

where $C_{En} = \frac{2\pi\epsilon}{\ln\left(\frac{D_{TSV}}{d_{CNT}}\right)}$ with D_{TSV} as the diameter of the via and d_{CNT} is the diameter of a single SW-CNT.

Similarly, $C_{Ef} = \frac{2\pi\epsilon}{\ln\left(\frac{2D_{TSV}}{d_{CNT}}\right)}$. n_w and n_H are the number of nanotubes across width and length respectively;

since we have considered a circular via for our modeling, we can approximate that $n_w = n_H = \sqrt{n_{CNT}}$.

Using these equations, we can obtain the parasitics for the electrical model shown in Fig. 3.

4.2 Electrical circuit model of MW-CNT-based TSV

For MW-CNTs, we considered a set of specifications to calculate the parasitic values and obtain the equivalent electrical model. The only difference between the electrical circuit model of SW-CNT-based TSV and MW-CNT-based TSV is that MW-CNTs have an additional parasitic in the form of kinetic inductance. This is shown in Fig. 4.

The kinetic inductance of the MW-CNTs are given by

$$L_K = \frac{h}{4ne^2\nu_F} \quad (16)$$

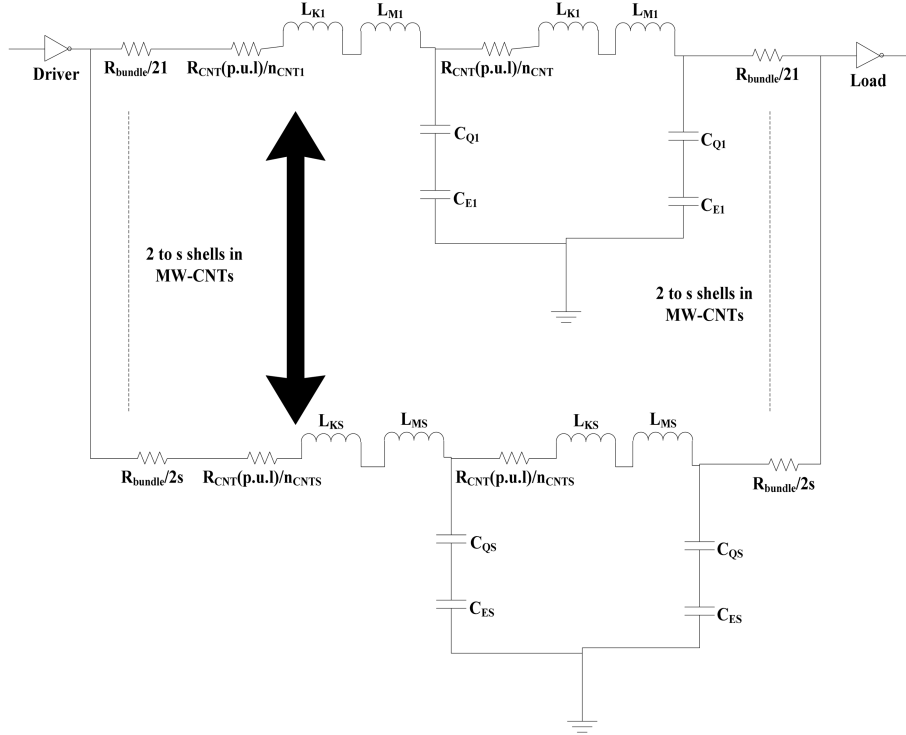


Fig. 4 Electrical model of MW-CNT

where n is the number of CNTs in the bundle.

This model is used along with the TSV substrates shown in Fig. 3 to obtain the equivalent electrical model for MW-CNTs.

5. Simulation results

In this section we consider two different case studies, one each for SW-CNT- and MW-CNT-based TSVs. Different via dimensions, CNT diameter and number of CNTs in the bundle were used in each case study. We studied the performance of the model as in Fig. 3 by calculating the S-parameters. Delay was also calculated using the TDR measurements. An eye diagram shows the density of the eye to perform a time domain analysis of the model. Finally, we compared the performance of SW-CNT-based TSV with MW-CNT-based TSV.

5.1 Case study 1

In this case we used SW-CNTs in the TSV. We considered the height and diameter of the via to be $15 \mu\text{m}$ and $3 \mu\text{m}$ respectively and the TSV pitch to be $20 \mu\text{m}$. The distance between the CNT bundles in the via and the ground plane is equal to the TSV pitch because we used a coplanar waveguide fashion to perform the S-parameter measurement. The diameter of the CNT is 2 nm and

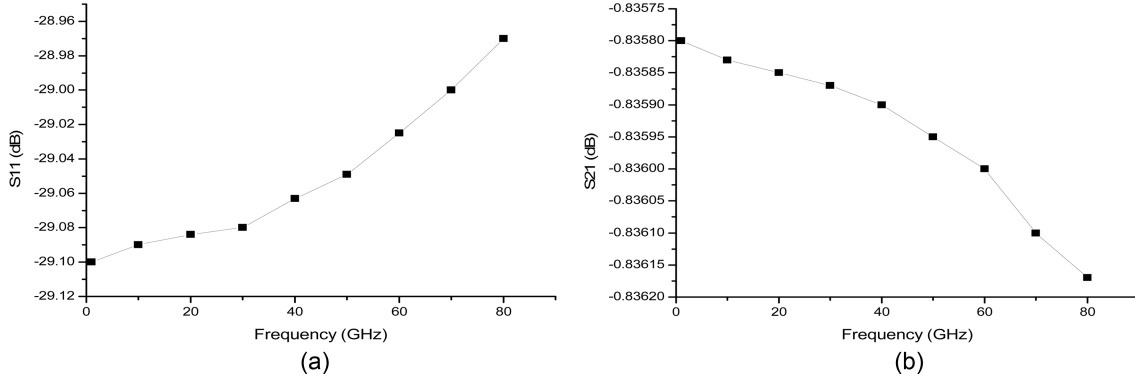


Fig. 4 SW-CNT-based TSV S -parameter measurement: (a) S_{11} parameter, (b) S_{21} parameter

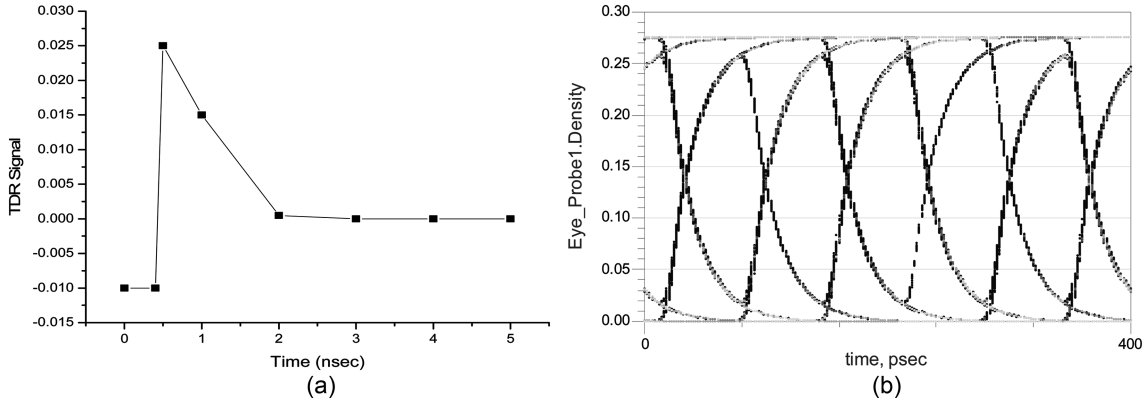


Fig. 5 SW-CNT-based TSV time domain measurement: (a) TDR measurement, (b) eye diagram

the number of CNTs in the bundle is 18761 which were obtained by assuming that CNTs occupy the complete area of a TSV and that a small percentage of these CNTs in the bundle are conducting. Fig. 4 shows the input port reflection represented by S_{11} parameter and the output port transmission by S_{21} parameter.

The S_{11} measurement shows that the input port reflection at high frequencies of the order of 75 GHz is -29 dB and the S_{21} measurement at frequencies of the order of 75 GHz is -0.84 dB. This shows that SW-CNTs have a very low input port reflection loss and high output port transmission. Fig. 5 shows the RC-interconnect delay of SW-CNT-based TSV by TDR analysis and the throughput by eye diagram analysis for high data rates on the order of 15 to 25 Gbps.

The TDR measurements show us that the rise time for SW-CNT is 1.5 nsec, which decreases the time delay in SW-CNT TSV; the eye diagram has good width and height of the eye for high data rates, thereby confirming the high throughput of SW-CNT-based TSVs.

5.2 Case study 2

In this case we used MW-CNTs in the TSV. We considered the height and diameter of the via to be $90 \mu\text{m}$ and $75 \mu\text{m}$ respectively and the TSV pitch to be $150 \mu\text{m}$. The distance between CNT

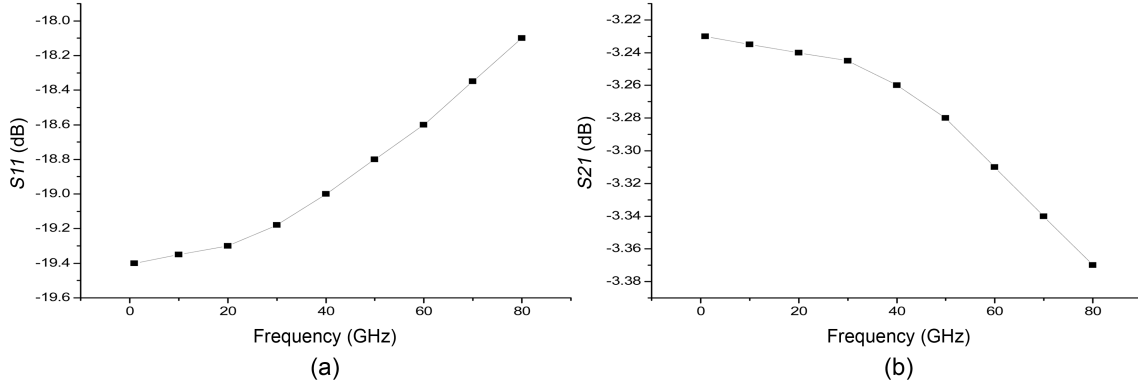


Fig. 6 MW-CNT-based TSV S -parameter measurement: (a) S_{11} parameter, (b) S_{21} parameter

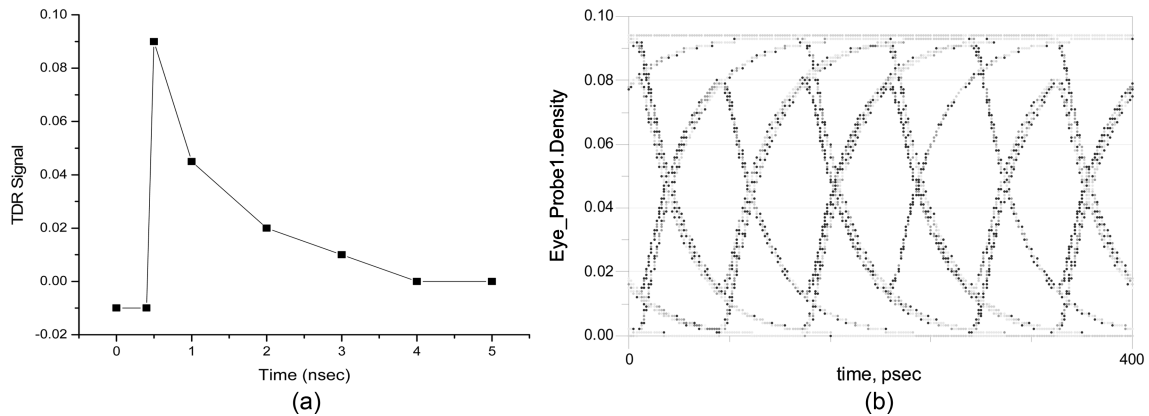


Fig. 7 MW-CNT-based TSV time domain measurement: (a) TDR measurement, (b) eye diagram

bundles in the via and the ground plane is equal to the TSV pitch because we used a coplanar waveguide fashion to perform the S -parameter measurement. The diameter of the CNT is 1 nm and the number of CNTs in the bundle is 37522, which is obtained by assuming that CNTs occupy the complete area of a TSV and that a small percentage of these CNTs in the bundle are conducting. The number of conducting multi-wall shells in the bundle is 75% of the total number of CNT bundles. Fig. 6 shows the input port reflection represented by S_{11} parameter and the output port transmission by S_{21} parameter.

The S_{11} measurement shows that the input port reflection at high frequencies of the order of 75 GHz is -18.4 dB and the S_{21} measurement at frequencies of the order of 75 GHz is -3.34 dB. This shows that MW-CNTs have a very low input port reflection loss and high output port transmission. Fig. 7 shows the RC-interconnect delay of MW-CNT-based TSV through TDR analysis and the throughput by eye diagram analysis for high data rates on the order of 15 to 25 Gbps.

The TDR measurements show us that the rise time for SW-CNT is 3.5 nsec which decreases the time delay in MW-CNT TSV; the eye diagram also has good width and height of the eye for high data rates, thereby confirming the high throughput of MW-CNT-based TSVs.

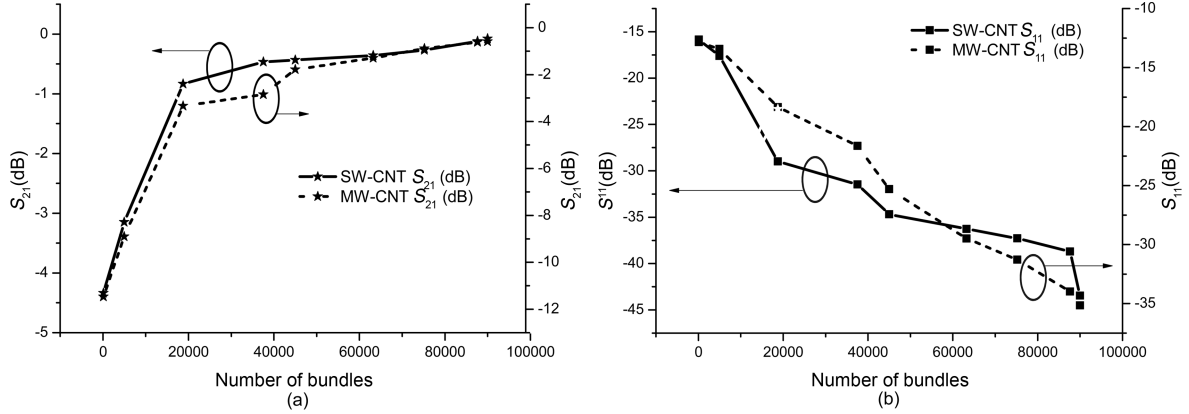


Fig. 8 S -parameter measurement for SW-CNT- and MW-CNT-based TSVs

5.3 Comparative study of SW-CNT and MW-CNT-based TSVs

A comparative study of the performances of SW-CNT- and MW-CNT-based TSVs was then performed. We considered different via dimensions, CNT diameters and number of CNTs in the bundle along with the number of conducting multi-wall shells in the bundle. The S -parameter measurement was computed and Fig. 8 shows the S_{11} and S_{22} parameters for SW-CNT- and MW-CNT-based TSVs.

Fig. 8 shows that as the number of CNTs in the bundle increases, the S_{11} parameter decreases, thereby exhibiting a lower input port reflection loss, and S_{21} increases, exhibiting higher output port transmission of the input signal. Thus as the number of conducting channels increases, the parasitics in the electrical model decrease thereby increasing the functional electrical performance of the TSV.

6. Conclusions

This paper presents a substrate-dependent model for SW-CNT- and MW-CNT-based TSVs used in silicon-based 3-D integration for high-frequency RF applications. The CNT interconnect parasitics in the proposed electrical model are obtained using the equations presented in the paper; the substrate is modeled as a function of frequency. We have incorporated various factors that affect the TSV performance at high frequencies; we analyzed the electrical performance of TSVs by performing S -parameter analysis, TDR delay and eye diagram analysis. Finally, we performed a comparative study of the electrical functional performance of SW-CNT- and MW-CNT-based TSVs for high-frequency RF applications.

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References

- Avron, J.E., Elgart, A., Graf, G.M., Sadun, L. and Schnee, K. (2004), "Adiabatic charge pumping in open quantum systems", *Commun. Pur. Appl. Math.*, **57**(4), 528-561.
- Banerjee, K. and Srivastava, N. (2006), "Are carbon nanotubes the future of VLSI interconnections?", *Proceedings of the 43rd Annual Design Automation Conference*, San Fransisco, CA, July.
- Benabe, E. (1998), "Automated characterization of ceramic multi-layer capacitors", *The Proceedings of the 52nd Advanced RF Techniques Group Conference*, Rohnert Park, December.
- Burke, P.J. (2002), "Luttinger liquid theory as a model of the gigahertz electrical properties of carbon nanotube", *IEEE T. Nanotechnol.*, **1**(3), 129-144.
- Datta, S. (1995), *Electronic transport in mesoscopic systems*, Cambridge University Press, Cambridge, UK.
- Datta, S. (2004), "Electrical resistance: An atomistic view", *Nanotechnology*, **15**(7), S433-S451.
- Greenhouse, H. (1974), "Design of planar rectangular microelectronic inductors", *IEEE T. Parts, Hybrids, Packaging*, **10**(2), 101-109.
- Gupta, A., Kim, B., Kannan, S., Ahn, B. and Mohhamad, F. (2010), "Development of novel carbon nanotube TSV technology", *Proceedings of the 60th Electronic Components and Technologies Conference*, Las Vegas, June.
- Han, K.J., Swaminathan, M. and Bandyopadhyay, T. (2010), "Electromagnetic modeling of through-silicon via (TSV) interconnections using cylindrical modal basis functions", *IEEE T. Adv. Packaging*, **33**(4), 804-817.
- ITRS ORTC (2008), *International Technology Roadmap for Semiconductors*, A. Allan, Rev 1 (for 7/16 Public Convergence Prep.), San Francisco, July.
- Kannan, S., Gupta, A., Kim, B., Mohammed, F. and Ahn, B. (2010), "Analysis of carbon nanotube based through silicon via", *Proceedings of the 60th Electronic Components and Technologies Conference*, Las Vegas, June.
- Kim, B., Kannan, S., Gupta, A., Mohammed, F. and Ahn, B. (2010), "Development of carbon nanotube based through-silicon vias", *J. Nanotechnol. Eng. Med.*, **1**(2), 121-128.
- Lakshminarayanan, B., Gordon Jr., H.C. and Weller T.M. (2000), "A substrate-dependent CAD model for ceramic multilayer capacitors", *IEEE T. Microw. Theory Techniq.*, **48**(10), 1687-1693.
- Maher, J.P., Jacobsen, R.T. and Laferty, R.E. (1978), "High-frequency measurements of Q-factors of ceramic chip capacitors", *IEEE T. Compon. Hybrid. Manuf. Tech.*, **1**(3), 257-264.
- Naeemi, A. and Meindl J.D. (2009), *Carbon nan-otube electronics*, Series on Integrated Circuits and Systems, Springer, New York, NY.
- Pucel, R.A. (1981), "Design considerations for monolithic microwave circuits", *IEEE T. Microw. Theory Tech.*, **29**(6), 513-534.
- Steinhogel, W., Schindler, G., Steinlesberger, G., Traving, M. and Engelhardt, M. (2005), "Comprehensive study of the resistivity of copper wires with lateral dimensions 100 nm and smaller", *J. Appl. Phys.*, **97**(2), 61-67.
- Yu, Z. and Burke, P.J. (2005), "Microwave transport in metallic single-walled carbon nanotubes", *Nano Lett.*, **5**(7), 1403.
- Zhu, J., Yu, Y., Hou, F. and Chen, C. (2010), "Through silicon via technologies for interconnects in RF MEMS", *Microsyst. Technol.*, **16**(7), 1045-1049.